AF/2486
$
2700
#
17
9K
9-16-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANT'S APPEAL BRIEF TRANSMITTAL LETTER

APPLICANT:	Stefan PFAB	DOCKET NO:	P00,0365
SERIAL NO.:	09/486,908	ART UNIT:	2186
FILED:	May 11, 2000	EXAMINER:	M. Anderson
TITLE:	DATA STORAGE DEVICE WITH OVERLAPPED BUFFERING SCHEME		

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant is submitting herewith, in triplicate, Appellants' Brief Under 37 CFR 1.192 in support of the Notice of Appeal filed February 9, 2001. Also enclosed is a check for the $320.00 fee required by 37 CFR 1.17(c). Please charge any additional fees which may be due and owing or credit any overpayment to Deposit Account No. 501519. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Mark Bergner (Reg. No. 45,877)

Mark Bergner
SCHIFF HARDIN & WAITE
Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6473
Customer Number 26574
(312) 258-5779
Attorneys for Appellant

CERTIFICATE OF MAILING

I hereby certify that an original plus one copy of this correspondence are being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on September 5, 2003

Mark Bergner

Mark Bergner – Attorney for Appellant

#17

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANT'S MAIN BRIEF ON APPEAL

APPLICANT:	Stefan PFAB	DOCKET NO:	P00,0365
SERIAL NO.:	09/486,908	ART UNIT:	2186
FILED:	May 11, 2000	EXAMINER:	M. Anderson
TITLE:	DATA STORAGE DEVICE WITH OVERLAPPED BUFFERING SCHEME		

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.192, Appellant submits this Brief in support of the appeal of the above-referenced application, in triplicate, in support of the patentability of claims 1-7 and 9-14 finally rejected in the Office Action, dated April 4, 2003. A copy of all claim in the application, including the claims on appeal is attached as Appendix A, and a copy of the Final Office Action is attached as Appendix B. A Notice of Appeal was filed on August 6, 2003.

REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee, Infineon Technologies, a German corporation.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and no related interferences known to Appellant, Appellant's Assignee, or Appellant's legal representative.

STATUS OF CLAIMS

Claims 1-7 and 9-14 are on appeal; claims 8 and 15 were objected to but were indicated as being allowable if written in independent and including all limitations of the base claim and any intervening claims. The status of the claims is as follows:

Claims	Status
8, 15	Allowed/allowable
1-7 & 9-14	Rejected

The rejected claims were rejected as follows:

Claims / Section	35 U.S.C. Sec.	References / Notes
1-7, 9-14	§102(e) Anticipation	• Pawlowski (U.S. Patent No. 5,787,475).

A copy of Pawlowski is attached as Amendment C.

STATUS OF AMENDMENTS

Amendment B was filed on March 26, 2003 and contained minor amendments to claims 6-8. These amendments were entered and made of record; these and the other claims of record formed the basis for the Final Office Action of April 4, 2003.

SUMMARY OF THE INVENTION

A data storage device must be able to read out stored data as quickly as possible. The slow data storage devices that are usually employed as program memories are usually not able to output their data as fast as modern program-controlled units can process them. Fast, static RAMs are therefore often employed as buffer memories (Caches). These Caches make it possible that the program-controlled unit does not always have to retrieve the required

data from the slow program memory but can often obtain them from the fast Cache. 1/7-19.

When a program section utilizing these memories have branch commands or other non-linear execution, however, the command to be executed after a branch may not be available in the Cache, and thus the slow program memory must continue to be accessed in these cases as previously. 1/20-2. Furthermore, the command that is to be retrieved from the program memory after a branch is often not completely contained in the data that are output by the program memory in response to a data output request. In such cases, two read accesses onto the program memory are required in order to be able to obtain the data representing the next command. This is significant, since approximately every third command in typical programs is a branch instruction. 1/28-2/7.

Data caches are typically structured to have a limited number of start addresses by which they can be accessed (e.g., every eighth byte), and a request for data must access the data cache using only one of the start addresses (e.g., on an eight-byte boundary). The data cache responds to a single access request by providing data located between the start address provided and the next available start address (e.g., start address + 0 to start address + 7). The present invention addresses this problem by providing a faster way of accessing this memory when branches are used in programs. It accomplishes this by making the distance between the start addresses smaller than the amount of data that is output in response to a data output request. 2/13-16. For example, the start addresses could be on an eight-byte boundary, but the data cache would respond to a single access request by outputting sixteen

bytes: start address + 0 to start address + 15. This helps to frequently limit data requests to a single access and therby reduce the time required for successive commands after branches, etc. 2/17-24.

ISSUES

The issue on appeal is whether the subject matter of claims 1-7 and 9-14 is anticipated under 35 U.S.C. §102(e) as being anticipated by Pawlowski (U.S. Patent No. 5, 787,475).

GROUPING OF CLAIMS

The claims on appeal include two independent claims (claims 1 and 9) and thirteen dependent claims (2-7). Since the basis in dispute for the rejection of the claims revolves around elements of independent claims 1 and 9, the patentability of the dependent claims stands or falls together with the patentability of independent claims 1 and 9.

ARGUMENT

ARGUMENT–Anticipation by Pawlowski

Examiner's Position: Pawlowski anticipates claims 1 and 9 because selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data in response to the data output request.

The Examiner, in the OA, pp. 3-4, indicated that Pawlowski discloses all of the elements of claims 1 and 9 as follows:

> a data storage device (main memory) (4/5-15) comprising:
>
> memory cells having stored data with selectable output addresses (4/34-45, 54-60, and figure 1, item 14), wherein the specific starting address provided by a request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the requested data and outputs

the requested data with cache lines, which are considered to be the selected output start address;

wherein the storage device (main memory) responds to a data output request (peripheral device) by outputting the stored data beginning with a selected output start address (4/34-45 and 5/66 - 6/10 ; and 6/19-35, 50-59), wherein the specific starting address provided by the request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the request data, and outputting the requested data with cache lines or consecutive cache lines, which are considered to be the selected output start address;

wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data in response to the data output request (6/30-35; 7/5-25; 9/56 – 10/15; 11/45-58, and 11/64 – 12/8). Data retrieved by the I/O controller to determine which cache line of data contains the beginning portion of address requested by the peripheral from the memory. If this beginning portion of the address is in the first cache line, then the data output to requested data by the first cache line. However, if the retriever determines that a next consecutive cache line contains the beginning portion of the requested data, the retriever increments the starting address and uses the incremented starting address to request the consecutive cache lines of data from memory. In all situations, a first cache line of consecutive cache lines, the data stored in the neighboring starting address is less than the output address since if the portion of the starting address provided by the requested data is in the first cache line, the output transfers to requested data by first cache line; and if it is greater than the first cache line, the output transfers by two consecutive cache lines.

In response to the Appellant's arguments in Amendment B, the Examiner maintained the rejection and stated, on p 6 of the OA:

> With respect to independent claims 1 and 9, the Applicant alleges that Pawlowski does not teach outputting an amount of data larger than the amount between neighboring output start addresses. The

> Examiner believes that Pawlowski still reads upon the claim language because it still outputs/transfers the prefetched cache line response to the first request. The desired data is repeatedly referred by Pawlowski as "the requested data" even though it may require a prefetch transfer. As recited in column 2, lines 30-35, a peripheral may request less than a cache line of data in one transaction and greater than a multiple number of cache lines of data in another transaction.

Appellant's Position: Pawlowski does not anticipate the present invention because the device of Pawlowski, in response to a data output request, outputs an amount of data that <u>corresponds to</u> the amount of data that can be stored between neighboring output start addresses, and does not output an amount of data <u>greater than</u> the amount of data that can be stored between neighboring output start addresses.

The last element of claim one requires that the data storage device is configured such that:

> [the] selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request

Or, stated another way, when a data output request is provided to the device, it can output an amount of data larger than the amount of data between neighboring output start addresses that the device can be addressed by.

This is not the way that Pawlowski operates. In Pawlowski, the main memory 14 is segmented into a plurality of addressable cache lines 18 (4/55-56). If another system component (e.g., the I/O module 24) wants to read out data stored in the main memory 14, it has to address the main memory 14 using the start address of one of the cache lines 18, and will receive the contents of a complete cache line (see, e.g., 6/15-19 and 50-59).

Therefore, the main memory 14 of Pawlowski is a data storage device comprising the feature that the selectable output start addresses are spaced from one another such that the amount of data that can be stored between neighboring output start address corresponds to the amount of data output in response to a data output request.

Pawlowski does not permit the access of the data storage device in amounts other than entire cache lines. According to Pawlowski, "All data transfers over the system bus must generally comprise an entire cache line worth of data." 4/59-60. Since the addressability of the cache memory 14 is only permitted at the beginning of the cache lines, it is only possible, according to Pawlowski, to get an amount of data *equal* to the spacing between neighboring start addresses per each request. In the relevant portions cited by the Examiner, e.g., 7/15-25, a "prefetch" of data beyond a single cache line may be performed, but this involves making a second or multiple requests of the memory: "... the data retriever may request a next consecutive cache line of data from main memory if the I/O controller has directed a second prefetch." 7/58-60.

The present invention primarily permits an overlap of the memory regions that can be retrieved based on the output start addresses of the memory device—i.e., multiple requests of the device may not be required when accessing an amount of memory larger than the spacing of the possible output start addresses, which provides a fundamental advantage in terms of speed.

Similarly, independent claim 9 requires the outputting of stored data from the data storage device that is greater in quantity than the space between the

neighboring output start addresses. Since Pawlowski only puts out a single cache line, and the neighboring output start addresses begin at the start of each cache line, Pawlowski does not anticipate independent claim 9 of the application.

The Examiner is improperly and inconsistently equating the combination of Pawlowski's I/O module *and* main memory with the "data storage device" of claims 1 and 9 in the present invention. The Examiner indicated in his Response to Arguments section of the OA on p. 6 that a peripheral of Pawlowski can request (and receive) some arbitrary amount of data, e.g., greater than one addressable cache line, with a single request, thereby anticipating claims 1 & 9 of the present invention.

While it is true that a combination of Pawlowski's I/O module *and* main memory module can provide an arbitrary amount of data greater than one addressable cache line, this still requires two accesses to the main memory module itself, as discussed above. The "device" of the present invention is only properly equated with the main memory module of Pawlowski (as indicated by the Examiner on p. 3 under numbered paragraph 7, "Pawlowski discloses a data storage devices (main memory)..."); the I/O module of Pawlowski acts as a separate entity (as the Examiner calls out in line 3 of numbered paragraph 10 of the OA) that is between the memory and output terminals. The disadvantage of Pawloski's use of the I/O module and main memory is that it involves an extra step—the main memory can only be accessed in cache line chunks and on cache

line boundaries... it requires extra processing by the I/O module to discard extraneous data and concatenate data that spans cache line boundaries.

This is precisely the type of delay that the present invention seeks to address, i.e., requiring multiple accesses of the data storage device. Device claim 1 and method claim 9 both permit the access of more data in a single request than the distance between two start addresses. This is neither taught or suggested by Pawlowski.

For the above reasons, Appellants respectfully contend that the present invention is not anticipated by Pawlowski and request reversal of the Examiner on these grounds for rejection.

CONCLUSION

For the above reasons, Appellants respectfully submits that the Examiner is in error in law and in fact in rejecting claims 1-7 based on the teachings of the above-discussed references, and that the finality of the last office action was improper in light of the circumstances. Reversal of the rejection of all of those claims is justified, and the same is respectfully requested.

This Brief is accompanied by a check in the amount of $320.00, as required by 37 C.F.R. §1.17(c). If necessary, the Commissioner is hereby authorized to charge any additional fees which may be required to account No. 501519. Please note that the Advisory Action incorrectly states that the Notice of

Appeal was filed on June 12, 2000--the Notice of Appeal was, in fact, filed on July 12, 2000, hence applicants believe that no additional fee is due.

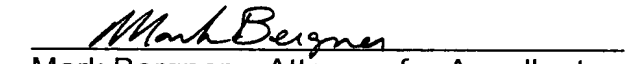
Respectfully submitted,


(Reg. No. 45,877)

Mark Bergner
SCHIFF HARDIN & WAITE
Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6473
Customer Number: 26574
(312) 258-5779
Attorneys for Appellant

CERTIFICATE OF MAILING

I hereby certify that an original and two copies of this correspondence are being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on September 5, 2003


Mark Bergner – Attorney for Appellant

APPENDIX A
CLAIMS INVOLVED IN THE APPEAL

1. A data storage device, comprising:

memory cells having stored data with selectable output addresses;

wherein said storage device responds to a data output request by outputting said stored data beginning with a selected output start address;

wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request.

2. A data storage device according to claim 1, wherein said selected output start address is determined utilizing address data applied to said data storage device.

3. A data storage device according to claim 2, wherein:

said selected output start address is determined by further utilizing adaptation data applied to said data storage device and;

said adaptation data is related both to said output start address to be employed and an address that is defined by said address data.

4. A data storage device according to claim 3, further comprising:

output terminals; and

an interface provided between memory cells of said data storage device and said output terminals;

wherein said adaptation data are used to control said interface.

5. A data storage device according to claim 4, wherein said interface comprises a multiplexer that is driven based on the adaptation data.

6. A data storage device according to claim 4, wherein data stored with an output start address selected from the group consisting of a first output start address and a second output start address are through-connected.

7. A data storage device according to claim 6, wherein said first output start address is an address that is represented by said address data applied to said data storage device.

8. A data storage device according to claim 6, wherein said second output start address is related to, but different from, said first output start address by a scope defined by a wiring of a multiplexer.

9. A method for outputting data from a data storage device, comprising the steps of:

receiving a data output request by said data storage device; and

outputting stored data in a quantity of data that is greater than a quantity of data that can be stored between neighboring output start addresses, and beginning said outputting of stored data with a selected output start address which is one of said output start addresses.

10. The method according to claim 9, further comprises the steps of:

applying address data to said data storage device; and

determining said selected output start address by utilizing said address data.

11. The method according to claim 10, further comprising the step of:

defining adaption data as an indicia related to said address data and said output start address;

applying said adaption data to said data storage device, wherein said step of determining said selected output start address utilizes said adaption data.

12. The method according to claim 11, further comprising the step of:

controlling, with said adaption data, an interface provided between memory cells of said data storage device and output terminals of said data storage device.

13. The method according to claim 12, further comprising the steps of:

controlling a multiplexer contained within said interface by applying said adaption data; and

through-connecting, via said multiplexer, data stored within said data storage device beginning with an address selected from the group consisting of a first output start address and a second output start address.

14. The method according to claim 13, further comprising the step of calculating said first output start address from said address data applied to said data storage device.

15. The method according to claim 13, further comprising the step of wiring said multiplexer so that said second output start address is related to, but different from, said first output start address by a scope defined by said wiring.

APPENDIX B
FINAL OFFICE ACTION

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/486,908	05/11/2000	STEFAN PFAB	P00.0365	9541

7590 04/04/2003

Schiff Hardin & White
Patent Department
7100 Sears Tower
CHICAGO, IL 60606-6473

EXAMINER
ANDERSON, MATTHEW D

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 04/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/486,908	Applicant(s) PFAB, STEFAN	
	Examiner Matthew D. Anderson	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-14* is/are rejected.

7)☒ Claim(s) *8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Amendment

2. In response to the amendment filed 3/26/03:

claims 6-8 have been amended, and the corresponding objections and USC 112 rejections have been withdrawn;

the title has been amended, and the corresponding objection has been withdrawn.

Allowable Subject Matter

3. Claims 8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: the prior art doe not teach or suggest the second output start address being related to, but different from, the first output start address by a scope defined by a wiring of the multiplexer.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-7 and 9-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Pawlowski (US Patent # 5,787,475).

7. With respect to claims 1 and 9, Pawlowski discloses a data storage device (main memory) (see column 4, lines 5-15) comprising:

memory cells having stored data with selectable output addresses (see column 4, lines 34-45, 54-60, and figure 1, item 14), wherein the specific starting address provided by a request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the requested data and outputs the requested data with cache lines, which are considered to be the selected output start address;

wherein the storage device (main memory) responds to a data output request (peripheral device) by outputting the stored data beginning with a selected output start address (see column 4, lines 34-45 and column 5, line 66 to column 6, lines 10; and column 6, lines 19-35 and 50-59), wherein the specific starting address provided by the request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the request data, and outputting the requested data with cache lines or consecutive cache lines, which are considered to be the selected output start address;

wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data in response to the data output request (see column 6 lines 30-35; column 7, lines 15-25; column 9 line 56 to column 10, line 15; column 11, lines 45-58, and column 11, line 64 to column 12, line 8). Data retrieved by the I/O controller to determine which cache line of data contains the beginning portion of address requested by the peripheral from the memory. If this beginning portion of the address is in the first cache line, then the data output to requested data by the first cache line. However, if the retriever determines that a next consecutive cache line contains the beginning portion of the requested data, the retriever increments the starting address and uses the incremented starting address to request the consecutive cache lines of data from memory. In all situations, a first cache line of consecutive cache lines, the data stored in the neighboring starting address is less than the output address since if the portion of the starting address provided by the requested data is in the first cache line, the output transfers to requested data by first cache line; and if it is greater than the first cache line, the output transfers by two consecutive cache lines.

8. With respect to claims 2 and 10, Pawlowski discloses a the selected output start address (beginning portion of started address for outputting the data requested by a cache line) is determined utilizing address data (peripheral device) applied to the data storage device (main memory) (see column 4, lines 34-45 and column 5, line 66 to column 6, line 10).

9. With respect to claims 3 and 11, Pawlowski discloses:

the selected output start address is determined by further utilizing adaptation data (data retriever) applied to the data storage (main memory) (see column 9, lines 22-42; and column 9, line 64 to column 10 line 15);

the adaptation data (data retriever) is related both to the output start address to be employed and an address that is defined by the address data (peripheral device) (see column 6, lines 30-35).

10. With respect to claims 4 and 12, Pawlowski discloses:

output terminals (main memory output terminals) (see figure 1, items 14 and 26);

an interface (I/O module) provided between memory cell of the data storage device (main memory) and the output terminals (see figure 1, items 14, 18, 24, 26, and figure 2, items 16, 42, 44, and column 6, lines 19-25).

11. With respect to claim 6, Pawlowski discloses using a prefetch system wherein the first cache line and second cache connected as a consecutive cache line for transferring the data to a requested data (peripheral device), and based on the beginning portion of the address provided by the requested data, if the starting address is greater than the first cache line, a consecutive line will be retrieved (see column 4, lines 54-60; column 5, line 66 to column 6, line 19, and column 7, lines 15-25). In other words, data stored with an output start address selected from the group consisting of a first output start address and a second output start address are through-connected.

12. With respect to claims 7 and 14, Pawlowski discloses the first output start address (beginning portion of the address provided by peripheral device for cache line output from the main memory) is an address that is represented by the address data (peripheral device) applied to the data storage device (main memory) (see column 5, line 59 to column 6, line 10).

13. With respect to claims 5 and 13, Pawlowski discloses a multiplexer that is driven based on the adaptation data, by showing in figure 2, data buffered from the data retriever is input into an I/O interface 44.

Response to Arguments

14. With respect to independent claims 1 and 9, the Applicant alleges that Pawlowski does not teach outputting an amount of data larger than the amount between neighboring output start addresses. The Examiner believes that Pawlowski still reads upon the claim language because it still outputs/transfers the prefetched cache line response to the first request. The desired data is repeatedly referred by Pawlowski as "the requested data" even though it may require a prefetch transfer. As recited in column 2, lines 30-35, a peripheral may request less than a cache line of data in one transaction and greater than a multiple number of cache lines of data in another transaction.

15. Because of the reasons given above, the rejections to claims 1-7 and 9-14 are maintained.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar data access systems.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (703) 306-59[illegible]. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications. Matt (703)746-5703

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MDA

Matthew D. Anderson
April 3, 2003

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

APPENDIX C
RELEVANT REFERENCES